WE CLAIM:

1. A circuit arrangement for sampling a logic data signal, comprising:

a first timer adapted to time a first time interval;

a delay timer coupled to the first timer and adapted to time a delay time interval initiated from the start of the first time interval;

a second timer coupled to the delay timer and adapted to time a second time interval initiated at the end of the delay time interval;

a coincidence circuit having an input terminal for receiving the logic data signal, an output terminal, and an enable terminal coupled to the second timer, the coincidence circuit adapted to pass a sample of digital event pulses comprising the logic data signal from the input terminal to the output terminal during the second time interval.

2. The circuit arrangement of claim 1, wherein the first timer is a binary count register having N+1 bits, the delay timer is a latch register having N bits, and the binary count register and latch register are coupled to a comparator circuit, and the comparator circuit adapted to initiate the second timer when the value of the binary count register and the value of the latch register are equivalent.

3. The circuit arrangement of claim 2, wherein the delay timer is adapted to pseudo-randomly vary the delay time interval.

4. The circuit arrangement of claim 3, wherein the delay timer is adapted to select the delay time interval from a finite set of discrete times.

5. The circuit arrangement of claim 3, wherein the latch register is a latching shift register.

6. The circuit arrangement of claim 5, further comprising a pseudo-random number generator coupled to the latch register, the pseudo-random number generator having less bits than the latch register and the pseudo-random number generator adapted to seed the latch register.

7. The circuit arrangement of claim 6, wherein the latching shift register is a round robin latch.

8. The circuit arrangement of claim 7, wherein the second timer is a second binary counter having M+1 bits, M being less than or equal to N.

9. The circuit arrangement of claim 8, wherein the first timer is adapted to time a series of periodic first time intervals.

10. The circuit arrangement of claim 9, wherein the delay timer is adapted to determine and time a new delay time interval for each first time interval in the series of first time intervals.

11. The circuit arrangement of claim 10, further comprising a counting circuit coupled to the output terminal of the coincidence circuit, the counting circuit adapted to accumulate a count of the digital event pulses in the sample.

12. The circuit arrangement of claim 11, wherein the counting circuit is reset responsive to the first timer.

13. A circuit arrangement for sampling a plurality of digital event pulses, comprising:

a first timer adapted to time a plurality of base time intervals;

a second timer adapted to generate a sampling window signal for a sampling window time interval, the sampling window time interval being a shorter time than any of the base time intervals;

a sample window initiate circuit coupled to the first timer and adapted to start the second timer at a pseudo-random time within each of the plurality of base time intervals; and

a sampler circuit coupled to the second timer and arranged to receive the plurality of digital event pulses and to pass a sample of digital event pulses responsive to the sampling window signal.

14. The circuit arrangement of claim 13, further comprising a counting circuit coupled to the sampler circuit, the counting circuit adapted to accumulate a count of the sample of digital event pulses.

15. The circuit arrangement of claim 14, wherein the counting circuit is a digital counter.

16. The circuit arrangement of claim 14, wherein the counting circuit further comprises a capacitor coupled through a transistor to a constant current source, the transistor being responsive to each of the digital event pulses to pass a substantially fixed amount of charge from the constant current source to the capacitor.

17. The circuit arrangement of claim 15, wherein the first timer is a binary counter having N+1 bits, and the second timer is a binary counter having M+1 bits, M being less than or equal to N.

18. The circuit arrangement of claim 17, wherein the first and second timers are adapted to count clock cycles, and the pseudo-random time being a discrete binary value of first timer.

19. The circuit arrangement of claim 18, wherein the sampling window initiate circuit comprises a pseudo-random number generator having K bits coupled to a shift register having N bits, the shift register arranged to receive and shift binary pseudo-random numbers from the pseudo-random number generator to form N bit pseudo-random numbers, whereby K is less than or equal to N.

20. The circuit arrangement of claim 19, wherein the shift register is a round robin latch.

21. The circuit arrangement of claim 20, wherein the overflow bit of the first timer is coupled to the counting circuit, the counting circuit adapted to reset responsive to the overflow bit of the first timer.

22. A method for sampling a logic data signal, comprising:

receiving a plurality of digital event pulses characterizing the logic data signal during each of a series of base time intervals;

applying a sampling window signal for a sample window time interval beginning at a pseudo-random time during each of a series of base time intervals;

selecting a subset of digital event pulses during application of the sampling window signal; and

accumulating a count of the subset digital event pulses.

23. The method of claim 22, further comprising:

timing each base time interval with a base time binary counter, the base time binary counter adapted to count clock cycles; and

timing the sample window time interval with a sample window binary counter, the sample window binary counter adapted to count clock cycles.

24. The method of claim 23, further comprising:

seeding a round robin latch with a pseudo-random number generator, the round robin latch having a length of N bits, the base time counter having a length of N+1 bits, and the pseudo-random number generator having fewer bits than the round robin latch;

shifting round robin latch bit values and populating all bits of the round robin latch;

forming an N bit pseudo-random number in the round robin latch; and

initiating timing of the sample window time interval when a value of the base time binary counter is equivalent to a value of the round robin latch.

25. The method of claim 24, further comprising resetting the count of the subset of digital event pulses accumulated at the end of each base time interval.

26. A circuit arrangement to sample a logic data signal, comprising:

means for receiving a plurality of digital event pulses characterizing the logic data signal during each of a series of base time intervals;

means for applying a sampling window signal for a sample window time interval beginning at a pseudo-random time during each of a series of base time intervals;

means for selecting a subset of digital event pulses during application of the sampling window signal; and

means for accumulating a count of the subset digital event pulses.